What is claimed is:

[Claim 1] 1. A voltage regulator circuit comprising:

an amplifier circuit comprising a first receiving terminal and a second receiving terminal for receiving a reference voltage and a feedback voltage respectively, the amplifier circuit outputting a driving voltage according to the reference voltage, the feedback voltage, and an enable signal;

an output transistor comprising three terminals electrically connected to the amplifier circuit, an output node, and a first voltage source respectively, the output transistor outputting a regulated voltage at the output node according to the driving voltage output by the amplifier and a voltage provided by the first voltage source;

a first discharge transistor comprising three terminals electrically connected to a reverse enable signal, the output node, and a feedback node respectively, the first discharge transistor controlling whether or not the output node is electrically connected to the feedback node according to the reverse enable signal, wherein the feedback node is electrically connected to the second receiving terminal of the amplifier circuit for providing the amplifier circuit with the feedback voltage;

a second discharge transistor comprising three terminals electrically connected to the reverse enable signal, the feedback node, and a second voltage source, the first discharge transistor controlling whether or not the feedback node is electrically connected to the second voltage source according to the reverse enable signal; and

a loading module electrically connected to the output node, the feedback node, and the second voltage source.

[Claim 2] 2. The voltage regulator circuit of claim 1 further comprising at least a bypass capacitor electrically connected to the second receiving terminal of the amplifier circuit.

[Claim 3] 3. The voltage regulator circuit of claim 1 wherein the three terminals of each transistor comprise a gate, a drain, and a source, the gate of the output transistor is electrically connected to the amplifier circuit, the drain of the output transistor is electrically connected to the output node, the source of the output transistor is electrically connected to the first voltage source, the gate of the first discharge transistor is electrically connected to the reverse enable signal, the drain of the first discharge transistor is electrically connected to the output node, the source of the first discharge transistor is electrically connected to the feedback node, the gate of the second discharge transistor is electrically connected to the reverse enable signal, the drain of the second discharge transistor is electrically connected to the feedback node, and the source of the second discharge transistor is electrically connected to the second voltage source .

[Claim 4] 4. The voltage regulator circuit of claim 3 further comprising a terminative transistor, whose gate, drain, and source are electrically connected to the enable signal, the gate of the output transistor, and the first voltage source respectively, wherein the terminative transistor controls whether or not the driving voltage is electrically connected to the first voltage source according to the enable signal.

[Claim 5] 5. The voltage regulator circuit of claim 4 wherein when the enable signal disables the operation of the amplifier circuit and turns on the terminative transistor, the terminative transistor controls the driving voltage to turn off the output transistor to stop the output transistor from outputting the output voltage to the output node.

[Claim 6] 6. The voltage regulator circuit of claim 4 wherein the first discharge transistor and the second discharge transistor are N-channel MOS (NMOS) transistors, and the output transistor and the terminative transistor are P-channel MOS (PMOS) transistors.

[Claim 7] 7. The voltage regulator circuit of claim 3 wherein the loading module comprises:

a loading capacitor connected to the output node and the second voltage source;

a first loading resistor connected to the output node and the feedback node; and

a second loading resistor connected to the feedback node and the second voltage source.

[Claim 8] 8. The voltage regulator circuit of claim 1 further comprising an inverter electrically connected to the gate of the first discharge transistor and the gate of the second discharge transistor for transforming the enable signal into the reverse enable signal and for outputting the reverse enable signal to the first discharge transistor and the second discharge transistor.

[Claim 9] 9. The voltage regulator circuit of claim 1 wherein the first voltage source is used for providing a high voltage level, and the second voltage source is used for providing a ground voltage or a low voltage level.

[Claim 10] 10. The voltage regulator circuit of claim 9 wherein when the enable signal disables the operation of the amplifier circuit, the driving voltage is used for turning off the output transistor to stop the output transistor from outputting the output voltage to the output node.

[Claim 11] 11. The voltage regulator circuit of claim 9 wherein when the enable signal disables the operation of the amplifier circuit, the reverse enable signal is used for turning on the first discharge transistor to connect the output node and the feedback node.

[Claim 12] 12. The voltage regulator circuit of claim 11 wherein when the enable signal disables the operation of the amplifier circuit, the reverse enable signal is used for turning on the second discharge transistor to connect the feedback node and the second voltage source so as to pull down the feedback voltage close to a voltage level provided by the second voltage source.

[Claim 13] 13. The voltage regulator circuit of claim 1 wherein the amplifier circuit is an operational amplifier or a differential amplifier.

[Claim 14] 14. A method for disabling a voltage regulator circuit, the voltage regulator circuit comprising an amplifier circuit for outputting a driving voltage according to a reference voltage, a feedback voltage on a feedback node, and an enable signal, an output transistor coupled among the amplifier circuit, a output node, and a first voltage source for regulating an output voltage at the output node; a first discharge transistor coupled among the enable signal, the output node, and a feedback node; and a second discharge transistor coupled among the enable signal, the feedback node, and a second voltage source; and the method comprising:

(a) utilizing the enable signal to disable the operation of the amplifier circuit for turning off the output transistor so as to stop the output transistor from outputting an output voltage at the output node;

(b) in step (a), utilizing the enable signal for turning on the first discharge transistor to connect the output node and the feedback node; and

(c) in step (a), utilizing the enable signal for turning on the second discharge transistor to connect the feedback node and the second voltage source.

[Claim 15] 15. The method of claim 14 wherein the amplifier circuit comprises a first receiving terminal and a second receiving terminal for respectively receiving the reference voltage and the feedback voltage, and the method further comprising:

(d) in step (c), pulling down the feedback voltage to the voltage level of the second voltage source when the second discharge transistor is turned on to connect the feedback node and the second voltage source.

[Claim 16] 16. The method of claim 14 wherein the regulator circuit further comprises a bypass capacitor electrically connected to the second receiving terminal of the amplifier circuit, and the method further comprises:

(e) in step (d), utilizing the bypass capacitor to suppress noise.

[Claim 17] 17. The method of claim 14 wherein the regulator circuit further comprises a terminative transistor coupled among the enable signal, the output transistor, and the first voltage source, and the method further comprises:

(f) in step (a), when the enable signal disables the amplifier circuit, turning on the terminative transistor for turning off the output transistor to stop the output node from being electrically connected to the first voltage source.

[Claim 18] 18. The method of claim 14 wherein the first voltage source is used for provide a high voltage level, and the second voltage source is used for providing a ground voltage or a low voltage level.

[Claim 19] 19. The method of claim 14 wherein the regulator circuit further comprises a loading module comprising:

a loading capacitor connected to the output node and the second voltage source;

a first loading resistor connected to the output node the feedback node; and

a second loading resistor connected to the feedback node and the second voltage source.

[Claim 20] 20. The method of claim 14 wherein the regulator circuit further comprises an inverter electrically connected to the first discharge transistor and the second discharge transistor for transforming the enable signal into the reverse enable signal, and the method further comprises:

(g) in step (b), utilizing the reverse enable signal for turning on the first discharge transistor to connect the output node and the feedback node; and

(h) in step (c), utilizing the reverse enable signal for turning on the second discharge transistor to connect the feedback node and the second voltage source.

[Claim 21] 21. The method of claim 14 wherein each of the output transistor, the first discharge transistor, and the second discharge transistor is a MOS transistor or a bipolar junction transistor (BJT).

[Claim 22] 22. The method of claim 21 wherein each of the first discharge transistor and the second discharge transistor is an N-channel MOS (NMOS) transistor, and the output transistor is a P-channel MOS (PMOS) transistor.

[Claim 23] 23. The method of claim 22 wherein the gate of the output transistor is electrically connected to the amplifier circuit, the drain of the output transistor is electrically connected to the first voltage source, the gate of the first discharge transistor is electrically connected to the enable signal, the drain of the first discharge transistor is electrically connected to the output node, the source of the first discharge transistor is electrically connected to the feedback node, the gate of the second discharge transistor is electrically connected to the enable signal, the drain of the second discharge transistor is electrically connected to the feedback node, and the source of the second discharge transistor is electrically connected to the second voltage source.

[Claim 24] 24. The method of claim 14 wherein the amplifier circuit is an operational amplifier or a differential amplifier.